What is claimed is:

1. A method of establishing a state of a phase-change memory, comprising:

writing a reset state as a high-resistance state by applying a reset current of about ten microamperes to several hundred microamperes to a phase-change layer of a phase-change memory cell for a period of from about 10 nanoseconds to about 100 nanoseconds; and

writing a set state as a low-resistance state by applying a set current of less than about several tens of microamperes to the phase-change layer for a period of from about 10 nanoseconds to about 100 nanoseconds.

2. The method of Claim 1, wherein the set current is from about 30 microamperes to about 50 microamperes, and the reset current is from about 60 microamperes to about 200 microamperes.

3. The method of Claim 1, wherein a reset resistance of the phase-change layer is from about 6 kΩ to about 20 kΩ.

4. The method of Claim 1, wherein the phase-change memory has a ratio of reset resistance to set resistance of from about 1.5 to about 3.

5. The method of Claim 1, wherein each of a rising time and a falling time of the reset current or the set current is from about 1 nanosecond to about 4 nanoseconds.

6. The method of Claim 1, wherein a current applied to the phase-change layer for reading the reset and/or the set states is from about 3 μA to about 6 μA and a time required for reading the reset and/or the set states is from about 5 nanoseconds to about 10 nanoseconds.

7. A method of driving a phase-change memory, the method comprising:

writing a set state by applying a set current of from about 30 μA to about 50 μA to a crystalline phase-change layer of a memory cell; and

writing a reset state by applying a reset current of from about 60 μA to about 200 μA to the phase-change layer, wherein the reset state is defined as a state where a resistance of the phase-change layer is greater than in the set.

8. The method of Claim 7, wherein a ratio of reset resistance to set resistance of the phase-change layer is from about 1.5 to about 3.

9. The method of Claim 7, wherein a current for reading the reset state and/or the set state is from about 3 μA to about 6 μA, and a period required for reading the reset state and/or the set state is from about 5 nanoseconds to about 10 nanoseconds.

10. The method of Claim 7, wherein a time required for writing the reset state and/or the set state is from about 10 nanoseconds to about 100 nanoseconds.

11. The method of Claim 7, wherein a reset resistance of the phase-change layer is from about 6 kΩ to about 20 kΩ.

12. The method of Claim 7, wherein a set resistance of the phase-change layer is from about 4 kΩ to about 6 kΩ.

13. A phase-change memory comprising:

a first electrode contact;

a phase-change layer on the first electrode contact; and

a second electrode contact on the phase-change layer,

wherein a set state is a state in which amorphous nuclei are formed in the phase-change layer that has a set resistance of from about 4 kΩ to 6 kΩ, and a reset state is a state in which the number and density of the amorphous nuclei are greater than in the set state and has a reset resistance of about 6 kΩ to 20 kΩ.

14. The memory of Claim 13, wherein a current for writing the reset state and/or the set state on the phase-change layer is from about 10 μA to about 200 μA, and a period required for writing the reset state and/or the set state from the phase-change layer is from about 10 nanoseconds to about 100 nanoseconds.

15. The memory of Claim 13, wherein a current for writing the set state in the phase-change layer is from about 30 μA to about 50 μA, and a current for writing the reset state in the phase-change layer is from about 60 μA to about 200 μA.

16. The memory of Claim 13, wherein a diameter of the first electrode contact to which the current is applied to write the reset and set states in the phase-change layer is from about 40 nanometers to about 70 nanometers.

17. The memory of Claim 13, wherein a rising time and a falling time for writing the reset state and/or the set state in the phase-change layer is from about 1 nanosecond to about 4 nanoseconds.

18. The memory of Claim 13, wherein a current for reading the reset state and/or the set state is from about 3 μA to about 6 μA, and a time required for reading the reset state and/or the set state is from about 5 nanoseconds to about 10 nanoseconds.

19. The memory of Claim 14, wherein a current for reading the reset state and/or the set state iss from about 3 μA to about 6 μA, and a time required for reading the reset state and/or the set state is from 5 nanoseconds to about 10 nanoseconds.

20. A phase-changeable memory device, comprising:

a phase change memory cell; and

a sense amplifier circuit configured to detect a change in resistance of the phase change memory cell from a first resistance associated with a first state of the phase change memory cell to a second resistance associate with a second state of the phase change memory cell, the second resistance being from about 1.5 to about 3 times the first resistance.

21. The phase-changeable memory device of Claim 20, wherein the first resistance is from about 4 kΩ to about 6 kΩ and the second resistance is from about 6 kΩ to about 20 kΩ.

22. The phase-changeable memory device of Claim 20, further comprising a set current source configured to provide a set write current of from about 30 μA to about 50 μA to the phase change memory cell.

23. The phase-changeable memory device of Claim 22, wherein the set write current is provided to the phase-change memory cell for from about 10 nanoseconds to about 100 nanoseconds.

24. The phase-changeable memory device of Claim 22, further comprising a reset current source configured to provide a reset write current of from about 60 μA to about 200 μA to the phase change memory cell.

25. The phase-changeable memory device of Claim 24, wherein the reset write current is provided to the phase-change memory cell for from about 10 nanoseconds to about 100 nanoseconds.

26. A phase change memory, comprising:

first and second electrode contacts;

a phase-change layer between the first and second electrode contacts, the phase change layer providing a first state established by a first number of amorphous nuclei in a crystalline matrix in a region adjacent an interface between the phase-change layer and the first electrode.

27. The phase change memory of Claim 26, wherein the phase change layer further provides a second state established by a second number of amorphous nuclei in a crystalline matrix in the region adjacent the interface between the phase-change layer and the first electrode, the second number being greater than the first number.

28. The phase change memory of Claim 27, wherein the first number of amorphous nuclei and the second number of amorphous nuclei provide a ratio of resistances of the phase-change layer of from about 1.5 to about 3.

29. The phase change memory cell of Claim 27, wherein the first state of the phase-change layer provides a resistance of the phase-change layer of from about 4 to about 6 kΩ and the second state the phase-change layer provides a resistance of the phase-change layer of from about 6 to about 20 kΩ.

30. The phase change memory cell of Claim 27, wherein a current for writing the first state or the second state on the phase-change layer is from about 10 μA to about 200 μA, and a period required for writing the first state or the second state from the phase-change layer is from about 10 nanoseconds to about 100 nanoseconds.

31. The phase change memory cell of Claim 27, wherein a current required for writing the first state in the phase-change layer is from about 30 μA to about 50 μA, and a current required for writing the second state in the phase-change layer is from about 60 μA to about 200 μA.

32. The phase change memory cell of Claim 27, wherein a diameter of the first electrode contact to which a current is applied to write the first and second states in the phase-change layer is from about 40 nanometers to about 70 nanometers.

33. The phase change memory cell of Claim 27, wherein a current for reading the first state and/or the second state is from about 3 μA to about 6 μA, and a time required for reading the first state and/or the second state is from about 5 nanoseconds to about 10 nanoseconds.

34. A method of operating a phase change memory, comprising:

establishing logic states in a phase change memory by controlling amorphous nucleation in a crystalline matrix of a phase-changeable material.

35. The method of Claim 34, wherein a first logic state is established by a first number of amorphous nuclei in the crystalline matrix and a second logic state is established by a second number of amorphous nuclei in the crystalline matrix in the, the second number being greater than the first number.

36. The method of Claim 35, wherein the first number of amorphous nuclei and the second number of amorphous nuclei provide a ratio of resistances of the phase-changeable material of from about 1.5 to about 3.

37. The method of Claim 35, wherein the first logic state provides a resistance of the phase-change layer of from about 4 kΩ to about 6 kΩ and the second logic state provides a resistance of the phase-change layer of from about 6 kΩ to about 20 kΩ.

38. The method of Claim 35, wherein controlling amorphous nucleation comprises controlling a current for writing the first logic state or the second logic state to be from about 10 μA to about 200 μA, and a period required for writing the first logic state or the second logic state to be from about 10 nanoseconds to about 100 nanoseconds.

39. The method of Claim 35, wherein controlling amorphous nucleation comprises:

controlling a current for writing the first logic state to be from about 30 μA to about 50 μA; and

controlling a current or writing the second logic state to be from about 60 μA to about 200 μA.

40. The method of Claim 35, wherein a diameter of the first electrode contact to which a current is applied to write the first and second logic states is from about 40 nanometers to about 70 nanometers.

41. The method of Claim 35, further comprising controlling a current for reading the first logic state and/or the second logic state to be from about 3 μA to about 6 μA, and a time for reading the first state and/or the second state to be from about 5 nanoseconds to about 10 nanoseconds.